



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,910	03/12/2004	Hong-Jyh Li	2004P50029US/I331.135.101	8291

7590 08/11/2006

Dicke, Billig & Czaja, PLLC
Suite 2250
Fifth Street Towers
100 South Fifth Street
Minneapolis, MN 55402

EXAMINER

HOANG, QUOC DINH

ART UNIT	PAPER NUMBER
----------	--------------

2818

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/799,910	Applicant(s) LI ET AL.	
	Examiner Quoc D. Hoang	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,7-15 and 17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,7-15 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 1-5, 7-15 and 17 are is withdrawn in view of the newly discovered reference(s) to Jeon. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Jeon et al., (US Pat No. 6,790,755 hereinafter "Jeon").

Regarding claim 15 Jeon teaches a transistor comprising;

a gate electrode (108) (col. 6, lines 50-55 and Fig. 1);

a high-k gate dielectric layer (110b) implanted with a species, the high-k material layer proximate the gate electrode (col. 3, lines 14-30, col. 7, lines 33-35 and Fig. 1);

a substrate (102) including active regions, the substrate proximate the high-k gate dielectric layer (col. 6, lines 50-55 and Fig. 1); and

a buffer (standard-K dielectric) layer (110c) implanted with a species between the high-k dielectric layer and the gate electrode (col. 3, lines 14-30, col. 7, lines 33-35 and Fig. 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-5, 7-14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeon et al., (US Pat No. 6,790,755 hereinafter "Jeon") in view of Kim et al., (US Pat No. 6,621,114 hereinafter "Kim").

Regarding claim 1, Jeon teaches a semiconductor device comprising;

a substrate (102) including active regions (col. 6, lines 50-55 and Fig. 1);

a high-k material layer (110b) implanted with a species, the high-k material layer proximate the substrate (col. 3, lines 14-30, col. 7, lines 33-35 and Fig. 1);

a gate electrode (108) proximate the high-k material layer (col. 6, lines 50-55 and Fig. 1); and

a buffer (standard-K dielectric) layer (110c) implanted with a species between the high-k material and the gate electrode (col. 3, lines 14-30, col. 7, lines 33-35 and Fig. 1).

Jeon teaches the substrate (102) including active regions, but does not teach the substrate including isolation regions.

However, Kim teaches a substrate (102) including isolation regions 121 (col. 5, lines 40-55 and Fig. 3). Since Jeon and Kim are all from the same field of endeavor, the purpose disclosed by Kim would have been recognized in the pertinent art of Jeon. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide isolation regions in order to electrically isolate transistor from other integrated circuit devices within the semiconductor substrate as taught by Kim, column 1, lines 50-55.

Regarding claim 2, Jeon teaches wherein a transistor (100) is formed from the substrate, the high-k material layer, and the gate electrode (col. 6, lines 50-55 and Fig. 1)

Regarding claim 3, Jeon teaches further comprising:

a pre-gate material layer (standard-k dielectric) (110a) between the substrate 102 and the high-k material layer (110b) (col. 6, lines 50-55 and Fig. 1).

Regarding claim 4, Jeon teaches wherein the pre-gate material layer comprises SiO₂ (col. 8, lines 1-2).

Regarding claim 5, Jeon teaches wherein the pre-gate material layer has a thickness up to about 10 Angstroms (col. 9, line 43).

Regarding claim 7, Jeon teaches wherein the buffer layer (110c) comprises SiN (col. 8, line 3).

Regarding claim 8, Jeon teaches wherein the buffer layer has a thickness of about 17 Angstroms (col. 9, line 43), but does not teach the buffer layer has a thickness of within the range of 10 to 200 Angstroms. Although Jeon's thickness of the buffer layer

is not the claimed range (10-200 Angstroms), this does not define patentable over Jeon since the thickness is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

Regarding claim 9, Jeon teaches wherein the species comprises nitrogen (col. 8, line 3).

Regarding claim 10, Jeon teaches wherein the high-k material layer (110b) comprises one of HfO_2 (col. 8, lines 15-31).

Regarding claim 11, Jeon teaches wherein the high-k material layer has a thickness of about 17 Angstroms (col. 9, line 43), but does not teach the high-k material layer has a thickness of within the range of 10 to 200 Angstroms. Although Jeon's thickness of the buffer layer is not the claimed range (10-200 Angstroms), this does not define patentable over Jeon since the thickness is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

Regarding claim 12, Jeon teaches 2 wherein the high-k material layer has an equivalent oxide thickness within the range of 10 to 20 Angstroms (col. 9, lines 15-22).

Regarding claim 13, Jeon teaches wherein a dose of the implanted species (nitrogen) of about 0 to 10 weight percent (col. 14, lines 57-58), but does not teach wherein a dose of the implanted species is within the range of 1×10^{13} ions/cm² to 1×10^{16} ions/cm². Although Jeon's dopant concentration is not the claimed range (1×10^{13} ions/cm² to 1×10^{16} ions/cm²), this does not define patentable over Jeon since the concentration is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art.

Regarding claim 14, Jeon does not teach the isolation regions comprise trench isolation regions.

However, Kim teaches wherein the isolation regions (121) comprise trench isolation regions (col. 1, line 55). Since Jeon and Kim are all from the same field of endeavor, the purpose disclosed by Kim would have been recognized in the pertinent art of Jeon. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide isolation regions in order to electrically isolate transistor from other integrated circuit devices within the semiconductor substrate as taught by Kim, column 1, lines 50-55.

Regarding claim 17 Jeon teaches the gate electrode (108), but does not teach wherein the gate electrode (108) comprises polysilicon.

However, Kim teaches wherein the gate electrode (118) comprises polysilicon (col. 2, line 10). Since Jeon and Kim are all from the same field of endeavor, the purpose disclosed by Kim would have been recognized in the pertinent art of Jeon. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide polysilicon gate electrode because polysilicon material is easily etch during the step of forming the gate electrode.

Conclusion


6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (571) 272-1780. The examiner can normally be reached on Monday-Friday from 8.00 AM to 5.00 PM.

Art Unit: 2818

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey can be reached on (571) 272-1835. The fax phone numbers of the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quoc Hoang
Patent examiner/AU 2818


08/05/2006